Sub-THz Transmitter Radio Integrated Circuits for Super high-speed 6G Mobile Communications

Bonghyuk Park
RF technology research section
ETRI
Daejeon, South Korea
bhpark@etri.re.kr

Sunwoo Kong
RF technology research section
ETRI
Daejeon, South Korea
swkong@etri.re.kr

Hui-Dong Lee
RF technology research section
ETRI
Daejeon, South Korea
leehd@etri.re.kr

Seunghun Wang
RF technology research section
ETRI
Daejeon, South Korea
wang@etri.re.kr

Seunghyun Jang
RF technology research section
ETRI
Daejeon, South Korea
damduk@etri.re.kr

Jung-Hwan Hwang
RF technology research section
ETRI
Daejeon, South Korea
jhhwang@etri.re.kr

***Abstract*— This paper presents system specifications from sub-THz RF system design, and based on these specifications, designed the RF transceiver architecture and frequency planning. Using the designed RF transceiver specifications, a 2-channel RF transmitter IC was designed using a 40nm CMOS process. The fabricated RFIC exhibits a frequency conversion gain of 7.83 dB, a 3-dB bandwidth of 12.4 GHz, and features gain variations of over 10 dB and a 360-degree phase variation capability. It shows a saturation power of 5.8 dBm based on 1-channel simulation.**

Keywords—6G, Sub-THz, radio intergrated circuits, phased-array, beamforming

I. INTRODUCTION

As the explosive increase in new services such as artificial intelligence, metaverse and XR has been a mainstream in cutting edge, the role of communications is becoming more significant than ever. In order to provide hologram display as a part of real-time services, extremely high data rate transmission, hundreds of times greater than current 5G system, will be essential. For example, 19.1 Gigapixel requires 1terabits per second(Tbps) [1]. A hologram display over a mobile device(one micro meter pixel size on a 6.7 inch display, i.e., 11.1 Gigapixel) form-factor requires at least 0.58 Tbps [2]. The wireless spectrum capable of supporting such data transmission rates is being considered with sub-THz carriers, which have bandwidths of over several tens of GHz, as the primary candidate frequencies [3]. However, due to significant path loss in the air, sub-THz frequency signals require compensation through a beamforming array using multiple antennas to secure the effective isotropic radiated power (EIRP). CMOS technology, known for its high integration, is advantageous in constituting the minimum units of complex beamforming systems. A waveguide-type antenna with high gain and strong forward directivity can be a solution for sub-THz systems, as it comprises more than a thousand elements in the array, and using power amplifiers with high output may lead to performance degradation due to heat generation. In this paper, we designed a 1024-channel system of the most easily implementable and straightforward RF beamforming structures. We also implemented the two-channel transmitter required for this structure using CMOS integrated circuits and presented the measured results. the need for research on low-loss RF front-end architectures.

II. SUB-THZ RF SYSTEM DESIGN

Recent research has mainly presented developments in sub-THz RF systems for high-speed transmission using planar patch antennas [4-5]. In this paper, for long-distance transmission, we consider high-gain waveguide antennas and design a 1024-channel array antenna system as shown in Fig. 1. The 8-channel beamformer modules are arranged horisontally, combining 4 of them to form 32 channels. Then, we arranged 32 of these modules vertically to create a 1024-channel array antenna system.

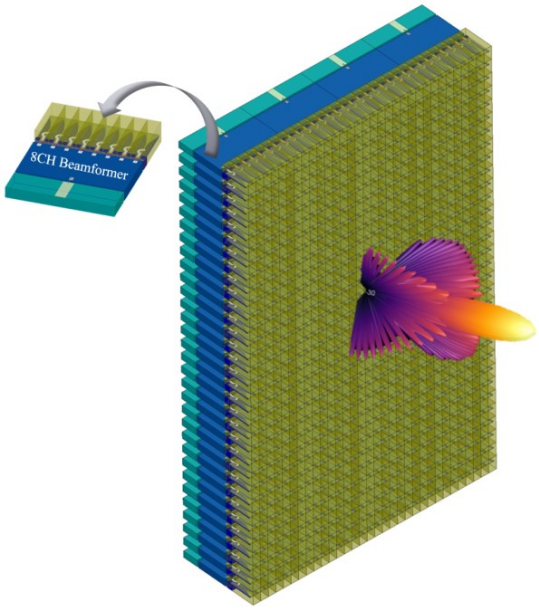
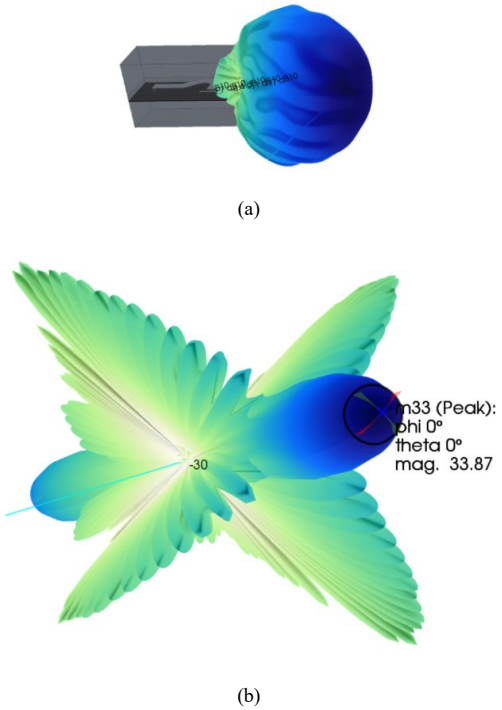


Fig. 1. 1,024-channel phased-array antenna system using high-gain waveguide antennas

Fig. 2(a) illustrates the characteristics of a sub-THz single-element waveguide antenna. The designed single antenna has a maximum gain of 7.87 dBi. After spacing the individual antennas vertically and horizontally by 0.5λ, the beam characteristics of the 1024-channel array antenna are presented in Fig. 2(b), showing a total array antenna maximum gain of 33.87 dBi. Even when the spacing between individual antennas is increased up to a maximum of 0.9λ, it was confirmed that the difference between the main-lobe and the largest side-lobe remains around 25.6 dB.



(a)

(b)

Fig. 2. Designed waveguide antenna beam patterns: (a) Single-antenna beam pattern, (b) 1024-channel array antenna beam pattern

The characteristics of the 32-channel array antenna's horizontal beam coverage design are depicted in Fig. 3. It demonstrates a maximum beam coverage of up to 140 degree.

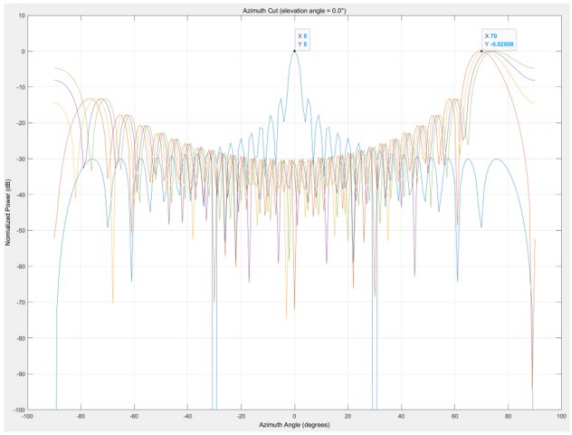


Fig. 3. Horizontal beam coverage of the 32-channel array antenna

The link budget was calculated using a 1024-channel array antenna designed to achieve a minimum distance of 150m with a 64QAM modulated signal, as shown in Table 1. The carrier frequency is 145GHz, and the 1FA (Frequency Allocation) channel has a bandwidth of 2.5GHz. The receiver's noise figure is 13dB, and the receiver's implementation loss is 4dB. Under these conditions, the power amplifier's output P1dB is 0dBm, satisfying the requirements. When simultaneously transmitting and receiving 4 FAs, a maximum data transmission rate of 45 Gbps can be achieved with the 64QAM signal.

TABLE I. LINK BUDGET FOR 64QAM@185 METERS

Parameter	Unit	Value	Note
Carrier frequency	GHz	145	
Bandwidth	GHz	10	4-FA(1-FA: 2.5GHz)
Tx single PA output	dBm	-12	Pavg = P1dB-PAPR(0dBm-12dB)
Tx power combining	dB	30	10*log(32x32)
Tx antenna gain	dBi	34	Designed array antenna gain
Tx EIRP	dBm	48	4dB implementation loss considered
Required SNR	dB	21.9	64QAM, AWGN channel
Rx NF	dB	13.0	Receiver cascaded noise figure
Rx antenna gain	dBi	34	Designed array antenna gain
Rx sensitivity	dBm	-39.1	10log(BW)+NF+SNR-174dBm
Modulation	bits/Symbol	6	8 for 256QAM, 6 for 64QAM, 4 for 16QAM
Spectral efficienty	bps/Hz	4.5	3/4 coding rate
Data rate	Gbps	45	4-FA(1-FA: 11.25Gbps)
Peak data rate	Gbps	360	Multi-beam(4)&Polarization(2) (MIMO)

Fig. 4 shows the transmission distance according to the modulation schemes. Simulations were performed under the condition that both the transmitter and receiver have a 1024-channel array. For the QPSK modulation scheme, the transmission distance was designed to be 410 meters, while for the 256QAM scheme, the achievable distance was 80 meters.

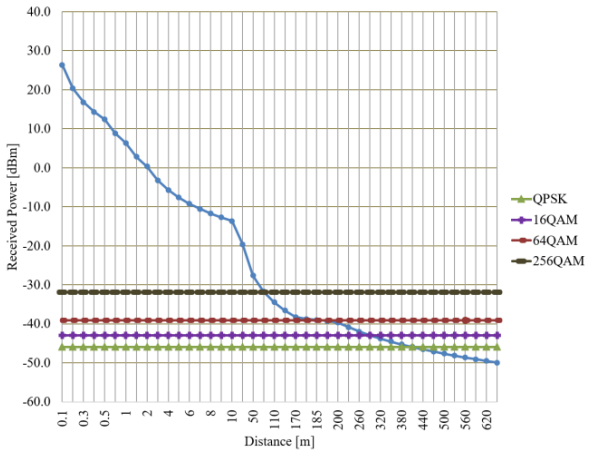


Fig. 4. Transmission distance on modulation

III. RF TRANSCEIVER ARCHITECTURE DESIGN

Fig. 5 illustrates the structure of a sub-THz RF Transceiver. It is designed with a heterodyne architecture, where the RF consists of four carrier frequencies at 141.25, 143.75, 146.25, and 148.75 GHz within the 140-150 GHz range. The Local Oscillator (LO) is supplied at 133 GHz, and the Intermediate Frequency (IF) comprises four channels centered around the 12 GHz frequency.

Fig. 6 depicts the structure of an IF Transceiver. With a center frequency of 12 GHz, it consists of an I, Q Modulator in the transmitting section and I, Q Demodulator in the receiving section, covering a bandwidth of 7 to 17 GHz. For each FA component, IF LO signals at 8.25, 10.75, 13.25, and 15.75 GHz are provided.

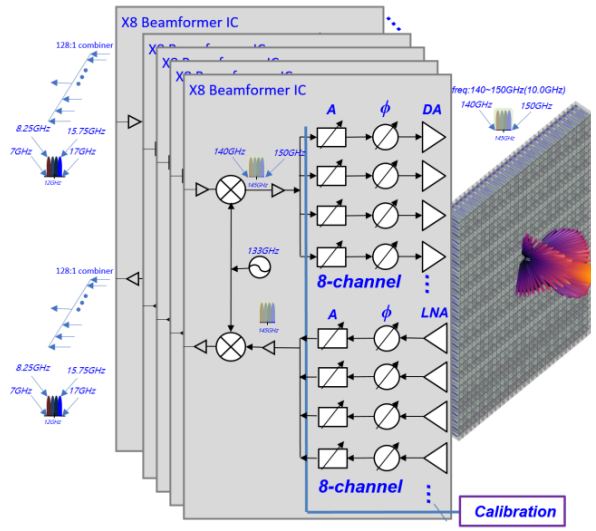


Fig. 5. Sub-THz RF transceiver architure

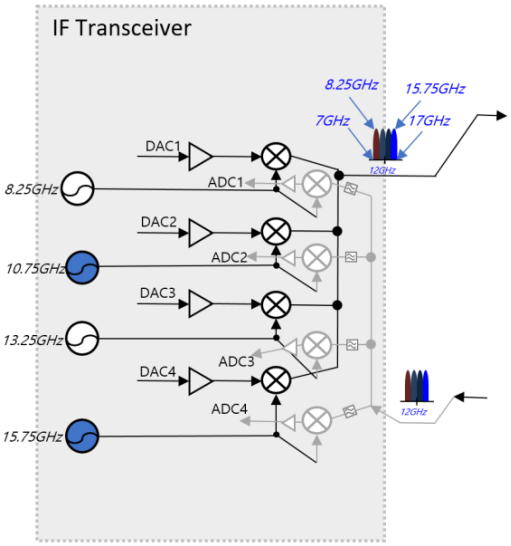
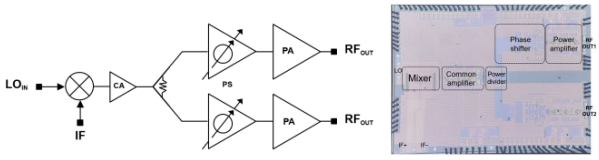


Fig. 6. Sub-THz IF transceiver architure

IV. Sub-THz Transmitter Integrated Circuits

The 2-channel transmitter integrated circuit is the basic unit of a beamforming multi-channel circuit that can be expanded to 4 channels or 8 channels in the future. As shown in the block diagram in Fig. 7, it includes all components necessary for constructing a multi-channel integrated circuit, such as a frequency up-converter, common amplifier (CA), power distributor, variable gain phase shifter (PS), and power amplifier (PA). Additionally, an LDO is integrated into the RF core to provide stable power supply, and an SPI is also integrated for controlling the phase and gain for each channel.

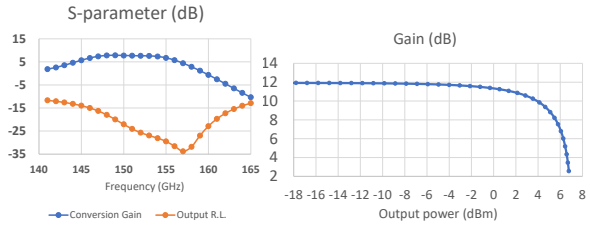
A passive mixer structure was selected for the up-conversion mixer to ensure a wide frequency bandwidth. This mixer combines a 136 GHz single-ended LO signal with a 5-15 GHz differential IF signal to output an RF signal in the 141-151 GHz range. Passive up-conversion mixers have a broad bandwidth but suffer from high insertion loss. Therefore, to sufficiently drive each channel, the RF signal generated at the output of the up-conversion mixer needs to be amplified. The common amplifier serves the purpose of amplifying each channel, and it is composed of variable gain phase shifters and power amplifiers to provide enough input power. The Wilkinson power splitter, located after the common amplifier stage, splits the input differential signal into two signals, directing each signal to its respective channel. The basic unit of the multi-channel integrated circuit is a single channel, which is constructed with a variable gain phase shifter and a power amplifier. The variable gain phase shifter, as seen in the measurement results of Fig. 8(c), can adjust both phase and gain within a single block, eliminating the need for additional gain adjustment blocks. This provides a size advantage [6]. In the case of the constructed 3-stage power amplifier, a G-max core was utilized to achieve high power gain [7]. The designed chip was fabricated using a 40nm CMOS process and has dimensions of 2600 x 1950 μm^2.



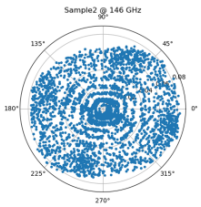
(a) (b)

Fig. 7. Sub-THz transmitter IC: (a) Block diagram, (b) Photograph

The simulation results for the 2-channel transmitter chip in Fig. 8 show a frequency conversion gain of 7.83 dB, a 3-dB bandwidth of 12.4 GHz, and the ability to achieve gain changes of over 10 dB along with a 360-degree phase variation. It has a saturation power of 5.8 dBm (based on 1-channel simulation).



(a) (b)



(c)

Fig. 8. 2-CH Sub-THz transmitter IC Disign results: (a) 2-CH S-parameter(Sim. result), (b) Power gain vs. Output power(Sim. result), (c) Constellation mea. results by gain/phase variation

V. Conclusion

In the present paper, we constructed a 2-channel beamforming transmitter integrated circuit using a CMOS process in the sub-THz frequency range. We measured the characteristics based on phase and gain variations. This IC can be used as a key RF component for 6G mobile communication that utilizes the sub-THz frequency range by configuring multi-channel ICs in the future.

Acknowledgment

This work was supported by Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (2021-0-00938, Development of THz RF core component)

References

[1] Xuewu Xu et al., "3D hogographic display and its data transmission requirement," in Proc. International Conf. Info, Photonics and Optical Commun., pp. 1-4, Oct. 2011

[2] Samsung Research, 6G White Paper: The next hyper-connected experience for all, July. 2020

[3] Samsung Research, 6G Spectrum: Expanding the frontier, May. 2022

[4] Mohamed Elkhouly, et al. "Fully integrated 2D Scalable TX/RX chipset for D-band phased-array-on-glass modules" 2022 International Solid-State Circuits Conference(ISSCC), IEEE 2022

[5] Amr Ahmed, et al. "A 140GHz scalable on-grid 8x8-element transmit-receive phased array with Up/Down converters and 64QAM/24Gbps data rates" 2023 IEEE Radio Frequency Integrated Circuits Symposium(RFIC), IEEE 2023

[6] Y. Kim and S. Hong, "A W-Band Vector Modulator Using Short-Channel Transistor Current Sources and Impedance Compensation Varactors," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 2, pp. 376-380.

[7] D. -W. Park, D. R. Utomo, B. Yun, H. U. Mahmood and S. -G. Lee, "A D-Band Power Amplifier in 65-nm CMOS by Adopting Simultaneous Output Power-and Gain-Matched Gmax-Core," in IEEE Access, vol. 9, pp. 99039-99049.