A Study of W-band FMCW Radar System in 65-nm CMOS technology for W-band Level Sensor

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***Abstract*—This paper present CMOS FMCW transceiver IC which is integrated in 65-nm CMOS technology. Transmitter consists of phase locked-loop(PLL), X4 frequency multiplier, divider, attenuator, power amplifier(PA) and receiver consists of low noise amplifier(LNA), mixer, LO drive amplifier and IF filter. In order to reduce ADC power consumption in the entire system, we designed a slow chirp generator with a chirp rising time of 1ms, allowing for the use of a low-resolution ADC by generating a low IF frequency. Transmitter achieves tuning range of 77~81 GHz and the phase noise -92 dBc/Hz @ 1MHz offset. The 3dB frequency of the IF filter is 3MHz, and the gain at 1MHz is 75dB. Entire system consumes 292 mW and 132 mW from a 1.2V and 2.5V power supply.**

Keywords—FMCW, W-band, Radar, CMOS

I. INTRODUCTION

Recently, W-band Frequency modulated continuous wave (FMCW) radar have been more and more widely used in level sensor system[1-2]. Due to the favorable duration in challenging conditions and the absence of signal scattering. In many level sensor systems, FMCW transceiver systems utilize high-speed chirp ICs designed for automotive applications. However, when creating an FMCW system using high-speed chirp ICs, the increased IF frequency necessitates a high-resolution ADC, leading to an increase in overall system power consumption. This paper proposes a slow chirp FMCW system with low phase noise characteristics and a wide output bandwidth using a 20 GHz Output Phase-Locked Loop(PLL) and an X4 frequency multiplier. The transmitter operates within the range of 77-81 GHz with an output power of 10 dBm. The phase noise is measured at -92 dBc/Hz @ 1 MHz offset. The receiver has a noise figure of 6dB. When combining the conversion loss of the IF mixer with the gain of the IF filter, the resulting IF filter gain is 75dB. When connecting the proposed system to a 25 dBi antenna and assuming a target's Radar Cross Section (RCS) of 10 dBsm, the system is capable of identifying targets up to a distance of 100 meters. Entire system consumes 292 mW and 132 mW from a 1.2V and 2.5V power supply. Utilization of a slow chirp system allows us to achieve a low IF frequency, thereby reducing the power consumption of the ADC and consequently lowering the overall power consumption of the entire system.

II. FMCW TRANSCEIVER ARCHITECTURE

A. Transmitter architecture

The block diagram of the designed FMCW chirp transceiver system is illustrated in Figure 1. The transmitter consists of a 20 GHz output Phase-Locked Loop, a frequency multiplier to quadruple the frequency, a Wilkinson divider, an attenuator, and a power amplifier.

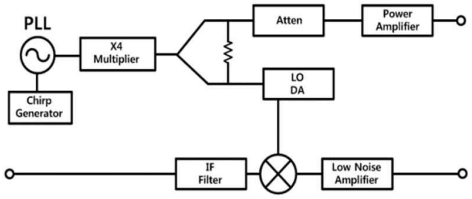

FIG 1. SCHEMATIC OF FMCW TRANSCEIVER

The phase-locked loop consists of a comparator, current pump, voltage-controlled oscillator, and delta-sigma modulator. It is configured with a frequency divider controller connected to the delta-sigma modulator of the phase-locked loop to generate a slow chirp signal. The LC-VCO within the phase-locked loop is constructed using a cross-coupled NMOS pair, a varactor, and a magnetically coupled transformer to simultaneously achieve low phase noise and a wide frequency tuning range[3-4]. In the system, a 10-bit delta-sigma modulator was designed. The chirp rising time was set to 1 ms, and with a 100 MHz reference, a total of 2000 steps were determined for the changing increments within the rising time Choosing the frequency ramp steps and loop filter bandwidth inappropriately can lead to an increase in frequency deviation, and excessively rapid responses can also escalate the deviation.

Frequency multiplier constructed by differential push pull topology. Push pull topology source and drain output voltage of pair of transistor is same frequency and opposite polarities[5]. A transformer was employed to combine the drain and source signals while minimizing the area. To design the frequency multiplier, the selection of gate bias in the push-pull topology is crucial. As indicated in equation (1), the gate

bias that maximizes gm' should be chosen. In this paper, a bias of 0.35V was selected.

$$\mathrm{gm}' = \frac{dgm}{dV_{GS}} = \frac{d^2 I_{DS}}{dV_{GS}{}^2} \quad (1)$$

By selecting the gate bias that results in the highest gm', and using a transformer to combine the signals between drain and source, the conversion loss of the frequency multiplier core is -5 dB. The TX output power at the final stage, including the power amplifier, is 10 dBm at 80 GHz.

B. Receiver architecture

The receiver consists of a low noise amplifier, LO drive amplifier, mixer, and IF filter. When designing an FMCW radar system using slow chirp, securing a good SNR in the low-frequency range is crucial due to the low IF frequency. To achieve this, the Noise Figure of the LNA was designed to be 6dB. Furthermore, importance of ensuring linearity in the LNA and mixer arises from the fact that receiver saturation due to leakage signals from transmitter mismatches can render signal demodulation impossible[6-7]. In this study, a passive mixer design was employed to ensure linearity. The LO signal for the mixer was supplied from the transmitter using a Wilkinson divider, and an LO driver amplifier was added to reduce conversion loss. The corner frequency of the IF filter is 3MHz, and the gain of the IF filter including the mixer's conversion loss is 75dB at 1MHz. Figure 2 shows the layout of the designed FMCW transceiver. It was designed using the CMOS 65-nm process and assembled as Chip-on-Board (CoB) on a TLY-5 substrate.

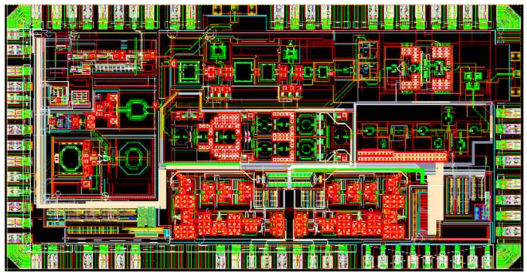

FIG 2. LAYOUT OF FMCW TRANSCEIVER

III. MEASUREMENT RESULT

A. Transmitter measurement

Figure 3 depicts the phase noise measurement results of the designed IC. The phase noise of the IC is -92 dBc/Hz @ 1MHz offset(at 80 GHz).

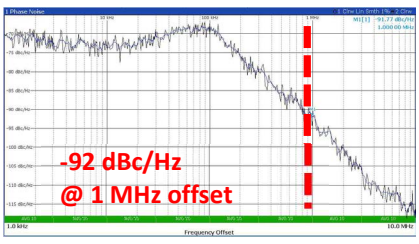

FIG 3. PHASE NOISE OF FMCW TRANSCEIVER

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The output power of the IC is 10 dBm at 80 GHz. Figure 4 shows the measured output of the IC's chirp signal compared to the ideal chirp signal. The chirp rising time is 1ms, and the next chirp signal starts after a 1ms idle period. When compared to the ideal reference, the measured deviation of the chirp signal is up to a maximum of 4 MHz. According to Equation 2, it can be understood that the FIF is related to the chirp rising time.

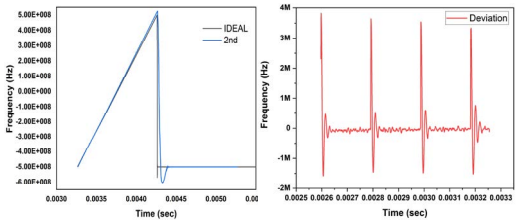

FIG 4. FMCW TRANSCEIVER OUTPUT SIGNAL VS IDEAL CHIRP SIGNAL AND MEASURED CHIRP DEVIATION

In this paper, with a chirp rising time of 1ms, even when assuming the target is 100 meters away, the FIF remains within 3 MHz, indicating a well-designed IF filter corner frequency.

$$\Delta F_{\boldsymbol{F}} \geq \frac{1}{T_C} \quad (2)$$

B. System measurement

To conduct measurements of the FMCW radar system, the IC was assembled using Chip-on-Board (CoB) technique on a TLY-5 substrate, and the system was assembled by connecting it to a horn antenna with a gain of 25 dBi. To account for various materials, measurements were conducted at different distances using reflectors with different Radar Cross Section(RCS) values. When calculating the system link budget, assuming an output power of 10 dBm, NF of 6 dB, antenna gain of 25 dBi, and target RCS of 10 dBsm, utilizing the IC developed in this paper enables identification up to 100 meters. Taking into account bonding losses at 80 GHz, as well as PCB transmission losses and cable losses, the experiment was conducted with a target located 50 meters away and having an RCS of 10 dBsm. Figure 5 presents the FMCW radar measurement setup and the output FFT results integrated with the DSP board.

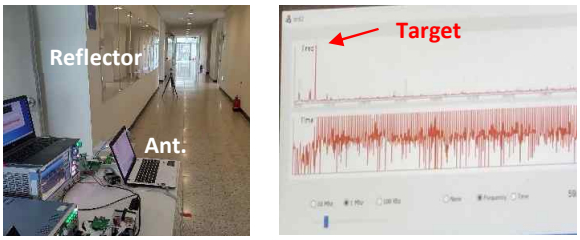

FIG 5. INTEGRATION EXPERIMENT WITH DSP BOARD

The measurement results indicate that the IF frequency of the target located 50 meters away is approximately 800 kHz. we can anticipate that the FIF of a target located 100 meters away would be approximately 1.6 MHz. The signal strength of the IF signal before signal processing is around -20 dBm,

which falls within the typical range of ADC input. Additionally, Tx leakage signals were also observed, which are believed to have resulted from mismatches between the IC, cables, and antenna. The leakage signals caused by mismatches can be removed through the DC offset cancellation circuit in the IF filter and DSP signal processing.

IV. Conclusion

We presented W-Band FMCW radar system IC with slow chirp generator, which are integrated in 65-nm CMOS technology. To simultaneously achieve low phase noise and a wide frequency tuning range, a topology utilizing a 20 GHz phase-locked loop and an X4 frequency multiplier was adopted . Designed W-Band FMCW radar IC operates within the output frequency range of 77-81 GHz, with a chirp rising time of 1ms. The phase noise of the output signal is -92 dBc/Hz @ 1MHz offset, and the deviation of the chirp signal is up to a maximum of 4 MHz. The output power is 10 dBm at 80 GHz, and the LNA noise figure is 6 dB. Utilizing the designed chip connected to a 25 dBi antenna and measuring a target with RCS of 10 dBsm, the calculated system link budget allows measurements up to 100 meters. By utilizing a slow chirp to produce a low IF frequency output, we have reduced the power consumption of the entire system through the use of low-resolution, low-power ADC.

Acknowledgment

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