A Design of High power 65nm CMOS 79GHz Power amplifier

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***Abstract*— This paper proposes power amplifier designs based on transformer matching network. The power amplifier has been designed in a 65nm CMOS technology, thus targeting ultra-precision radar and millimeter-wave applications. Their operating ranges are 77-81 GHz and the gain is 18.9 dB at center frequency. It provides a saturated output power of 14.5 dBm with the power-added efficiency (PAE) of 10.5%, and the output 1-dB gain-compressed power (P1dB) is 10.7 dBm with the PAE of 4.5% at 79 GHz, respectively.**

Keywords—CMOS, 65㎚, 79GHz, Radar, PA

I. INTRODUCTION

Radar is a system that uses radio waves to detect the distance of a target. It is a system that detects direction, angle, and speed, and has been used primarily in the fields of defense and aviation, but in recent years, there has been an explosion of demand in industries such as autonomous vehicles, ultra-precise level sensing, and IoT sensors.

The main bands for industrial leveling are X-band from 6 to 11 GHz and K-band from 24 to 29 GHz, and in recent years, W-band radar from 75 to 85 GHz has been used as demand for ultra-precise level sensing has exploded. The Table 1 below summarizes the propagation characteristics of each band. The table summarizes the propagation characteristics of each band. As you can see, as you move up to W-band, resolutions of several millimeters are possible. Therefore, this paper proposes an 79 GHz high-power CMOS power amplifier, which is required for ultra-precision level sensing radar systems.

TABLE I. LEVEL SENSING RESOLUTION BY FREQUENCY

Freq. Range	Band	Freq.	Wavelength(λ)
Low	C & X-band	6-11GHz	50-30mm(≒2~1.2-in.)
Mid	K-band	24~29GHz	~10mm(≒0.4-in.)
High	W-band	75-85GHz	4-3.5mm(≒0.15-in.)

II. DESIGN OF CMOS POWER AMPLIFIER

In ultra-precision radar, CMOS power amplifiers are one of the most challenging blocks due to the low breakdown voltage of the transistors and the losses in the monolithic matching network built on the silicon substrate. The requirements for power amplifiers in ultra-precision radar are high output power, high efficiency, small size, and reliability[1].

Accurate transistor models play a key role in designing millimeter-wave circuits. The size of the unit transistor is set after investigating the maximum oscillation frequency (F_{Max}) and maximum available gain (MAG) in relation to the unit gate width and number of fingers of the NMOS, respectively.

Larger unit gate widths improve MAG but decrease F_{Max} due to higher gate resistance. Also, the higher the number of fingers, the lower the F_{Max} value. Figure 1 shows the maximum available gain under different gate width conditions. The transistor had a unit finger width of 1.3 μm. The simulated MAG, biased to 0.75 V gate and 1.2 V drain, was 9.6 dB at 79 GHz.

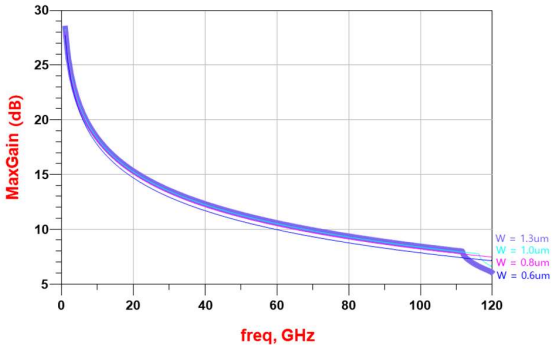

Fig. 1. MAG simulation results as gate width changes

A. *Selecting a unit cell for Power stage*

To verify the output power and efficiency, which are the key characteristics of a power amplifier, a load-pull simulation was performed. As shown in Figure 2, we can see that the P_{Max} and PAE_{Max} points at 79 GHz are different, and we chose Z_L = 5.4+j*2.1 and Z_S = 2.1+j*6.7 to realize a high-power amplifier. The core-cells were organized into 8 units to achieve an output power of 16.7dBm and a PAE of 14.48%.

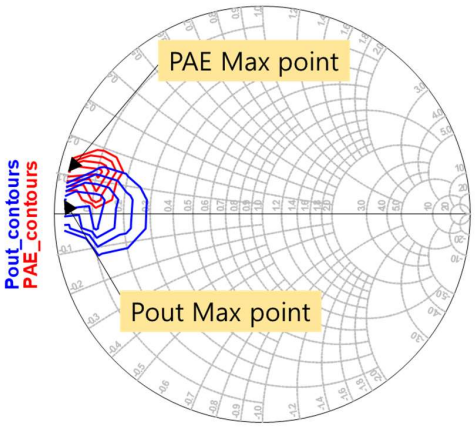

Fig. 2. Load-pull simulation result of power cell

B. *Transformer structure for high performance*

To design the compact and wideband CMOS power amplifier, a structure of power amplifier with transformer is considered. In addition, choke inductors at high frequencies are one of the most difficult to construct, which is unavoidable in a single ended circuit. However, if a transformer is used, the center tab acts as a virtual ground, eliminating the need to use a choke inductor and solving this problem. Therefore, in this paper, a matching network was constructed using a transformer for the core cell identified earlier. Figure 3 shows a schematic of a three stage Transformer-PA. It consists of two driver stage, power stage, and four matching networks for input, output, and two inter-stage, respectively.

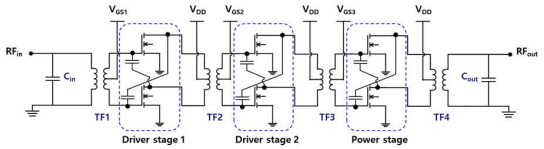

Fig. 3. Schematic of the proposed power amplifier

There are several key advantages to using transformers as a matching network.

First, second-harmonics can be eliminated for the following reasons. If the signal applied to the transformer is differential, as shown in Figure 4, the nonlinearity caused by even order harmonics can be eliminated, increasing efficiency. As shown in equation (1), Vout+ and Vout- are summed to give V_{OD}, which removes the even order harmonics.

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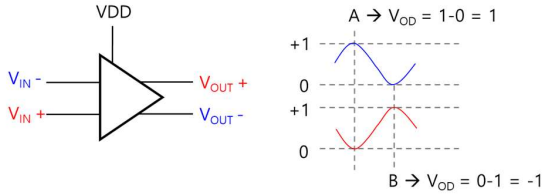

Fig. 4. Behavioral characteristics of differential amplifiers

$$V_{out+} = k_1V_{in} + k_2V_{in}^2 + k_3V_{in}^3 + \cdots$$

$$where\ , V_{in} = A\cos\omega$$

$$where, V_{out} = A\cos(2\omega_1) + \frac{k_2A^2}{2}(1+\cos(2\omega_1)) + \frac{k_3A^3}{4}(1+\cos(3\omega_1) + 3\cos(\omega_1) + \ldots$$

$$V_{out-} = k_1(-V_{in}) + k_2(-V_{in}^2) + k_3(-V_{in}^3) + \cdots$$

$$V_{OD} = 2k_1V_{in} + 2k_3V_{in}^3 + \cdots \quad (1)$$

Second, it is typically known for its low insertion loss compared to Pi-type matching networks.

Third, transformers at the input and output protect the circuit by discharging ESD.

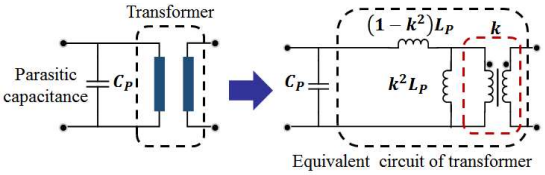

Fig. 5. Equivalent circuit of a transformer

Figure 5 shows a tuned transformer equivalent circuit. The inter-winding capacitance and parasitic board capacitance are not shown in this circuit. The transformer with capacitors is used as a parallel resonant device. The resonant frequency of a tuned transformer is given by

$$\omega_r = \frac{1}{\sqrt{(1-k^2)\cdot L_P \cdot C_P}} \quad (2)$$

where k is the coupling factor, L_P is the total primary inductance of the transformer, and C_P is the parasitic capacitance of the transistor. The effects of the inter-winding capacitance and the feeding-line inductance are also considered[1].

The transformers in the circuit were all precisely designed and simulated with the Advanced Design system (ADS) EM simulation tool. The inputs and outputs of the transformers in the metal stack were either metal 9 or metal 8. The center tap of the transformer was metal 7 and the bottom ground was metal 1, 2, and 3. The inductance and coupling factor were designed based on tradeoffs between impedance and power matching, gain, and bandwidth. The transformer was designed using vertical coupling between metal 9 and metal 8, which is more effective than a side-coupled design. The transformer also has a spiral shape, which has a higher Q factor than a square symmetrical shape. Figure 6 shows the designed interstage transformer and output transformer.

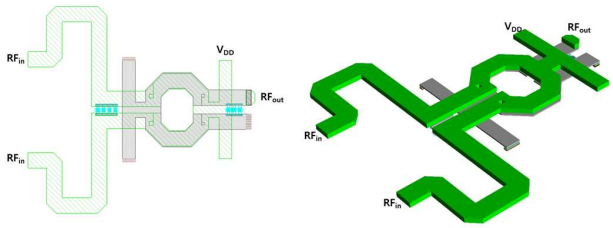

Fig. 6. Transformer layout used for output matching

At higher frequencies, the partially EM-simulated data and the fully EM-simulated data were different. Compared to the partial simulation results, we could see that the full simulation results were shifted to high frequencies, so we performed full EM simulation in the last step.

C. Circuits to eliminate oscillations

Because the transistors in a power amplifier have a very large area, the parasitic gate-to-drain capacitance is also very large, reaching hundreds of fF. High parasitic gate-to-drain capacitance adversely affects power gain and stability.

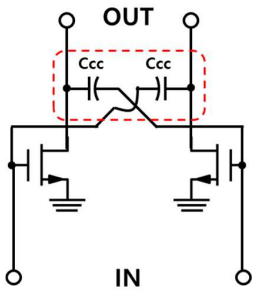

Fig. 7. Simplified cross-coupled capacitance schematic

Figure 7 shows a simplified circuit to illustrate a capacitive cross-coupled neuron. The capacitor *Ccc* between the cross-coupled gate and the opposite drain operates as -*Ccc* and offsets the parasitic gate-to-drain capacitance and improves oscillation.

D. Simulaion result of 79GHz Power amplifier

Figure 8 shows full layout of designed CMOS Transformer-PA which has 4 transformers and cross-coupled capacitor.

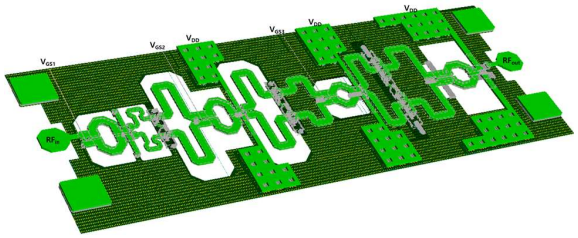

Fig. 8. Full layout of the designed power amplifier

The VDD and VGS in all stages are biased with 1.2 V and 0.75V, respectively.

In the fourth stage, eight transistor cells are used for parallel power combining to achieve the simulated output power of 14.5 dBm. Figure 9. shows the simulated S-parameters. And output P1dB from 77 GHz to 81 GHz as shown on Figure 10. The maximum gain of the PA is about 18.9 dB at 79 GHz and the gain variation within the operation band is less than 1.3 dB.

Also, the simulated minimum output P1dB of 10.2 dBm is observed at 81 GHz, while the P1dB variation within the operation band is less than 1.12 dB.

Furthermore, Figure 10. shows the simulated PAE of the PA, and the maximum PAE of 10.5% is observed at 79 GHz.

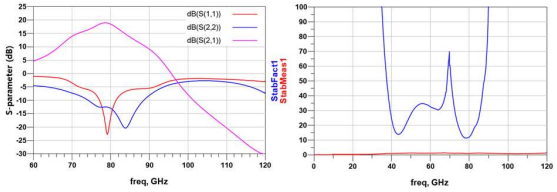

Fig. 9. S-parameter characteristics of the designed power amplifier

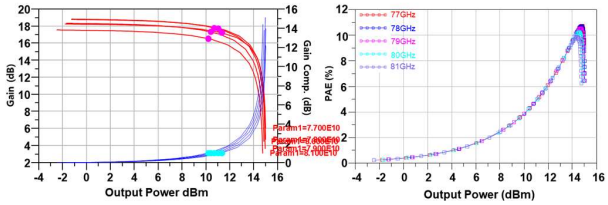

Fig. 10. Output power characteristics of the designed power amplifier

III. Conclusion

In this paper, a power amplifier for ultra-precision radar has been designed. It provides a saturated output power of 14.5 dBm with the PAE of 10.5%, and the P1dB is 10.7 dBm with the PAE of 4.5% at 79 GHz, respectively. The small-signal gain is 18.9 dB at center frequency. Such results in a 65nm CMOS process may apply to the development of precise results ultra-precision level sensing radar systems.

References

[1] Suk-Hui Lee, Ki-Jin Kim, Kwang-Ho Ahn and Sung-il Bang, “A Design of Power Amplifier for CMOS Crystal-less Wireless Connectivity,” ICTC , 2017.

[2] I. S. Jacobs and C. P. Bean, “Using capacitive cross coupling technique in RF low noise amplifiers and down-conversion mixer design,” in Proceedings of the 26th European Soild-State Circuits Conference, Stockholm, Sweden, September 2000.

[3] A. Rofougaran, J.Y-C.Chang, M. Rofougaran, A. A. Abidi, "A 1GHz CMOS RF front-end IC for a direct conversion wireless receiver ", IEEE J. Solid-State Circuits, July 1996, vol. 31, pp. 880-889.

[4] A. R. Shahani, D. K. Shaffer, and T. H. Lee, "A 12-mW Wide Dynamic Range CMOS Front-End for Portable GPS Receiver ", IEEE J. Solid-State Circuits, Dec 1997, vol. 32, pp. 2061-2069.

[5] K. C. Tsai and P. R. Gray, "A 1.9 GHz 1-W CMOS class-E power amplifier for wireless communications", *IEEE J. Solid-State Circuits*, vol. 34, pp. 962-969, July 1999.

[6] H. Chung et al., "Proof-of-concept demonstration of a 22-GHz vehicular communication system over an urban roadway testbed", *Proc. Int. Conf. Inf. Commun. Technol. Converg. (ICTC)*, pp. 857-859, Oct. 2020