Design of a K-Band Beamformer for Receiving Active Phased Array Anetennas for satellite communications

Duyong Seo
LIG NEX1
C4I R&D Laboratory
Pangyo, Korea
Duyong.seo@lignex1.com

Sangpill Lee
LIG NEX1
C4I R&D Laboratory
Pangyo, Korea
leesangpill@lignex1.com

Choongho Song
LIG NEX1
C4I R&D Laboratory
Pangyo, Korea
choonghosong@lignex1.com

Moonkyu Cho
Korea National University of Transportation
Dept. of Computer Engineering
Chungju-si, Korea
moonkyu.cho@ut.ac.kr

Seunghwan Jung
GRIT CIC
Seoul, Korea
sh.jung@gritcic.com

Abstract— In this paper, a Beamformer IC for receiving active phased-array antennas operating in the K-band for satellite communication was designed using the 65nm 1P9M CMOS process. The designed beamformer consists of a Low Noise Amplifier (LNA), Phase Shifter (PS), Loss Compensation Amplifier (LCA), Digital Step Attenuator (DSA), and LCA in that order. The input of the beamformer was initially designed in a single-ended structure, considering the antenna's interface, but later internal circuits were designed in a differential structure using balun to enhance noise cancellation.

The LNA consists of a total of 3 stages, and the final stage was designed as a buffer stage with matching for PS. Since the input of the beamformer is the input of LNA, it was designed in a single-ended structure and converted to a differential structure by balun. Even after a received signal went through the differential structure, performance degradation was inevitable due to mismatches. So, we matched the impedance by balun, cross-coupled capacitor that appears to be a negative capacitance for increasing stability and a degeneration inductor for noise matching. The designed LNA achieves a measured gain of 23.8 dB and a noise figure of 4.2 dB.

The phase value of the PS was made to be adjustable from 0 to 357.2° in increments of 2.8°, and three additional tuning bits were added. For phase changes below 11.25°, which are relatively small, a simplified T-type PS that removed the very small inductor and series switch transistor from a general T-type PS was used, and for phase changes above 22.5°, a modified bridged T-type PS that a capacitor was added on the control transistor side of the general bridged T-type PS was employed. As a result, the PS was able to reduce loss and parasitic capacitance, and enable wideband characteristic. Furthermore, the removal of the inductors enabled a smaller chip area.

The LCA for loss compensation consists of a 2-stage gain stage and a buffer stage for matching with the next stage. The 2-stage gain compensation structure with two general Cascode amplifier structure was designed.

The attenuation value of the designed DSA can be varied from o to 31.5 dB in 0.5 dB increments, and three 0.25 dB tuning bits were added. When the attenuation is below 2 dB, a simplified T-type attenuator structure was designed by removing the two very small series resistors from exiting T-type attenuator's input and output respectively. As a result, the control transistor also was unnecessary. For attenuation of 4 dB or more, a modified Pi-type attenuator structure was used to compensate for phase variation by adding a capacitor on the source side of the transistor in a shunt configuration, thus canceling out the pole and zero. For a 16 dB attenuator, two 8 dB attenuators were used for wideband characteristics.

The measured results show that beamformer gives the power gain of 30dB, OP1dB of 10dBm, IP1dB of -30dBm, and NF of 5.3dB. The total Beamformer consumes 92.5 mW from a 1.2 V supply and occupies 4,280 x 800 μm^2.

Keywords—CMOS, K-Band, Receiver, RX, Satellite, LNA, LCA, PS, DSA, Beamformer

[1] T. Kuo, Y. Lin, C. Chen and H. Wang, "A 40 GHz High Linearity Transmitter in 65 nm CMOS Technology with 32dBm OIP3," IEEE MTT-S International Microwave Symposium, Jun. 2019.

[2] Joon-Hyung Kim et.al., "High-Performance Broadband CMOS Low-Noise Amplifier with a Three-Winding Transformer for Broadband Matching," IEEE Radio Frequency Integrated Circuit Symposium, Jun. 2023.