Implementation of Single Chip 28 GHz SPDT Switch-less Front-end Circuits in a 65nm CMOS process

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***Abstract*— This paper presents the implementation results of a single-chip 28 GHz SPDT-less front-end IC for 5G mobile communication services. The focus of the present paper is on investigating the implementation performance of a low-loss RF front-end architecture eliminating the SPDT switch in a conventional front-end. According to the measurement results, the SPDT-less design shows negligible loss at the output stage and hence higher output power. The fabricated CMOS chip exhibits excellent performance, with a peak gain of 20.8 dB and a 3-dB bandwidth of 4 GHz (28 GHz – 32 GHz) in the Tx-mode. In Rx-mode, a wider bandwidth characteristic of 7.4 GHz (25.6 GHz – 33 GHz) and a peak gain of 18.9 dB are observed. The overall results demonstrate the potential of the SPDT-less front-end for efficient reception and future low-loss RF front-end designs**

Keywords—5G, 28GHz, mobile communication, FEM, front-end module, beamforming

I. Introduction

In recent years, significant efforts have been made to deploy fifth-generation (5G) mobile communication services [1-3, 6-8, 10-15] using the 28 GHz frequency-band[6-8, 10-13]. However, as the frequency increases, the power consumption for the signal amplification dramatically rises, highlighting the need for research on low-loss RF front-end architectures. In this paper, as part of these ongoing efforts, the implementation results of a single-chip 28 GHz SPDT (Single-Pole Double-Throw) switch-less front-end IC on a standard 65nm CMOS process are provided. By eliminating the SPDT switch required in a conventional RF front-end, as shown Fig. 1, the loss of the output stage of the SPDT-less front-end was negligible and, as a result, enhance the output power level[12].

II. SPDT Switch-less Front-End

The 28GHz SPDT-less front-end circuits have been designed on a standard CMOS 65nm process. As shown in Fig. 2(a), the power amplifier in the front-end has two-stage differential cascode structure and four neutralized capacitors. With the neutralized capacitors, the stability problem of the power amplifier is relieved[4-5]. For the input, output and inter-stage matchings, transformers are designed for small size and low loss. The structure of the LNA is illustrated in Fig. 2(b). The LNA has three-stage common-source structure with

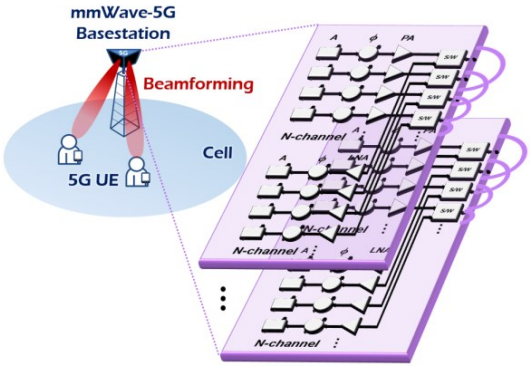
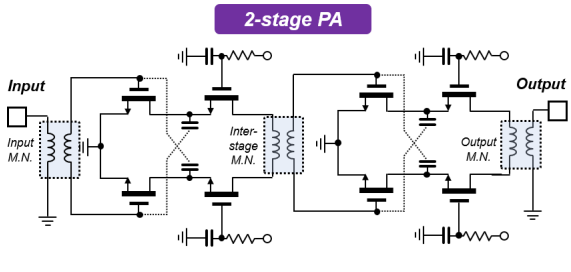
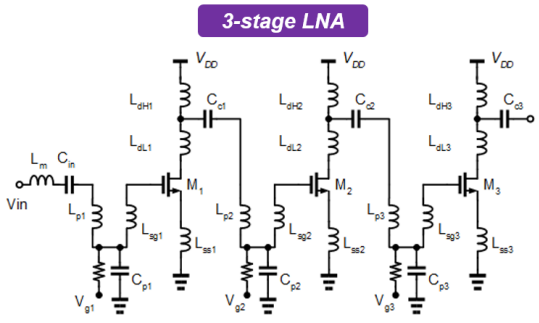


Fig. 1. RF front-ends in mmWave beamforming modules for 5G mobile communication

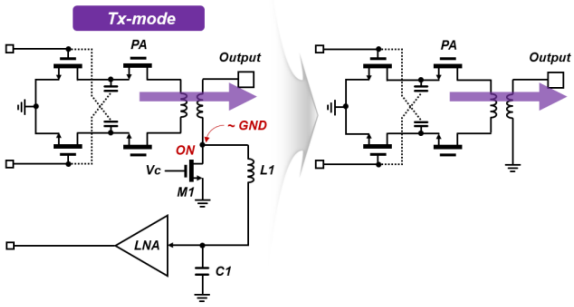


(a)

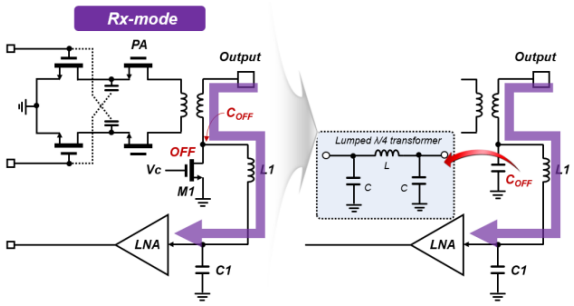


(b)

Fig. 2. Block diagrams: (a) power amplifer, (b) low-noise amplifer



(a)



(b)

Fig. 3. Operation principle of SPDT-less front-end circuits: (a)Tx-mode, (b) Rx-mode

several transformer matching circuits and transformer output load[7].

The architecture and basic operation principles of the SPDT-less front-end are depicted in Fig. 3[12]. By using the PA output transformer as one block of a transmit/receive(T/R) switch network and then eliminate a lossy SPDT switch, the T/R switching structure can be simple. For Tx-mode, M1 is ON and the one of the secondary winding of the PA output transformer is connected to GND, which is virtually the same architecture of the PA itself. For Rx-mode, M1 is OFF, the signal from the output PAD to the LNA input experiences the secondary winding of the PA output transformer and the C-L-C network consisting of C_{OFF} of M1, L1 and C1, as shown in Fig. 3(b). Since the C-L-C network is a λ/4 transformer, it can be used as a matching network for LNA input and reduce the number of LNA input matching components.

III. Measurement Results

The designed SPDT-less front-end chip has been fabricated in a CMOS 65nm process, and the size of the chip is 720μm x 910μm including PADs, as shown Fig. 4. The PADs in the middle of the chip are for additional GNDs.

Fig. 5 shows the measurement results of the Tx-mode of the chip. The PA was biased with VDD of 1.8V, 1.3V for cascode-stages, and 0.445V for the 1st and 2nd common-source stages, resulting in a quiescent current of 93 mA. The peak gain of 20.8 dB was observed at around 30 GHz with a 3-dB bandwidth of 4 GHz (28 GHz – 32 GHz). Overall, it was slightly optimized for frequencies slightly higher than 28 GHz. Although the Tx-mode front-end chip exhibits relatively broad frequency characteristics, it is necessary to achieve a

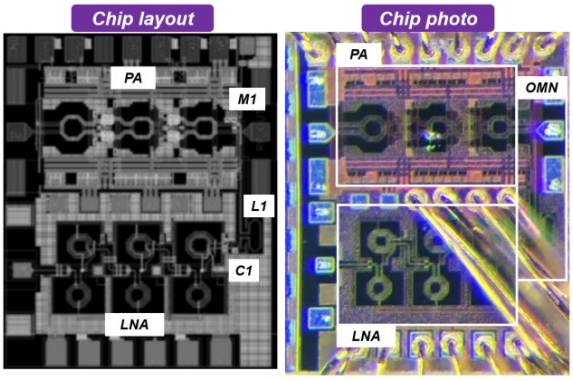
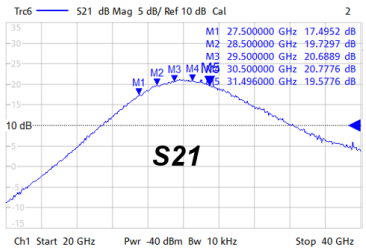
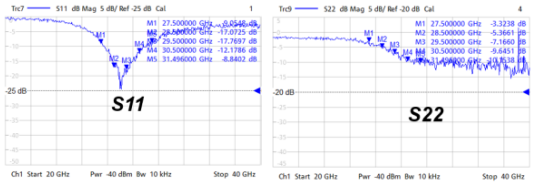


Fig. 4. Chip layout and photo graph of the 28 GHz CMOS SPDT-less front-end chip



(a)



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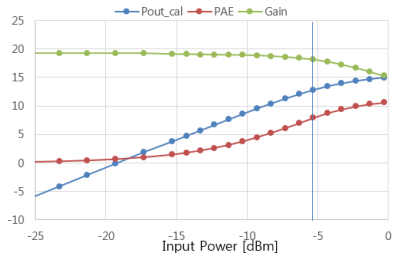
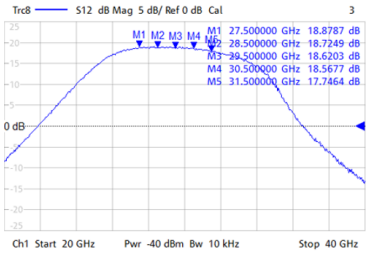


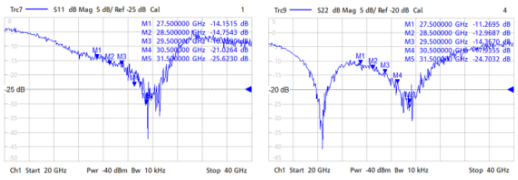
(c)

Fig. 5. Measurement results of the Tx-mode of the fabricated front-end chip: (a) S21, (b) S11 and S22, and (c) power, gain and PAE

wider bandwidth for the input/output matching of the power amplifier in order to provide more margin for PVT (process, voltage, temperature) variations. This is an important aspect to consider and will be addressed in future designs. To investigate the output power characteristics of the transmitter, a one-tone test was conducted, and the measurement results are presented in Fig. 5(c). The maximum efficiency exhibited was 11%, and the maximum output power was greater than 15.5 dBm. The gain was greater than 20.5 dB, but it showed a rapid decline in gain, resulting in a measured output P1dB of 12.5 dBm.



(a)



(b)

Fig. 6. Measurement results of the Rx-mode of the fabricated front-end chip: (a) S12, (b) S11 and S22

The measured S-parameter performance of the Rx-mode of the front-end chip is shown in Fig. 6. The receiver consumes 15 mA from a 1.2V supply. In Fig. 6(a), the measured Rx-mode gain is depicted. Compared to the Tx-mode, the receiver demonstrates a wider bandwidth characteristic with the 3-dB bandwidth of 7.4 GHz(25.6 GHz – 33.0 GHz) with a peak gain of 18.9 dB. Unfortunately, we were unable to measure the noise figure of the Rx-mode of the chip. The EM simulation provided the noise figure of the Rx-mode was around 5.4 dB, and the noise figure of the LNA itself was approximately 3 dB.

The summary of the measurement results of the fabricated 28 GHz SPDT-less CMOS front-end chip was shown in Table I.

TABLE I. PERFORMANCE SUMMARY

T/R Mode	**Fabricated SPDT-less 28GHz FEM chip**	
	Parameter	***Measurement***
Tx-mode	Frequency	28 GHz – 32 GHz
	Maximum gain	20.8 dB
	Input/Output return losses	< -8.8 dB (Input) < -5.4 dB (Output)
	Maximum output power	15.5 dBm
Rx-mode	Frequency	25.6 GHz – 33 GHz
	Maximum gain	18.9 dB
	Input/Output return losses	< -12 dB (Input) < -14 dB (Output)
	Noise figure[a]	5.4 dB

[a.] EM simulation result

IV. CONCLUSION

In the present paper, the implementation results of the 28 GHz SPDT-less front-end IC were provided and discussed. The Tx-mode of the chip exhibited the maximum output power of over 15.5 dBm, making it suitable for 5G mobile communication services. The Rx-mode demonstrated a wider bandwidth characteristic and a peak gain of 18.9 dB, indicating its potential for efficient reception in the designated frequency range. Further research is required to measure the noise figure of the Rx-mode, but the overall performance of the SPDT-less front-end chip highlights its potential for low-loss RF front-end architectures in future designs.

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